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EXAMINER

LI, AIMEE J

ART UNIT PAPER NUMBER

2183

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/843,178

Applicant(s)

GOSIOR ET AL.

Examiner

Aimee J Li

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. Claims 1-18 and new claims 19-20 have been considered. Claims 1-3 and 6-16 have been amended as per Applicant's request. New claims 19-20 have been added as per Applicant's request.

#### ***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 16 October 2004 and Three Month Extension of Time as filed 16 October 2004.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6-7, 9-10, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627.

5. Regarding claim 1, Parady has taught a programmable, single chip embedded processor system for input/output applications, comprising:

- a. A modular, multiple-bit, multithreaded processor core (see Fig.3) operable by at least four parallel and independent processor threads sharing common execution logic segmented into a multiple-stage processor pipeline (see Fig.3 and Col.3 lines 35-43). Here, the processor supports four threads, each with its own context (or state) using separate register files (see Col.3 lines 44-49).

- b. An instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set (41 of Fig.3),
  - c. A supervisory control unit (112 of Fig.3), controlled by at least one of said processor core threads, for examining the processor core state and for controlling the operations of said processor core (see Col.3 lines 57-65). Here, the thread switching logic monitors cache misses caused by a thread, and subsequently causes a thread switch. The thread switch is controlled by a current thread which can dictate which thread to switch to (see Col.3 lines 57-65).
  - d. A memory capable of storing data comprising instructions from said instruction set (see 152 of Fig.5),
  - e. A peripheral adaptor (178 of Fig.5/6) engaged with said processor core for transmitting input/output signals to and from said processor core (see Figs. 5 and 6).
6. Regarding claim 2, Parady has taught a system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage (see Col.3 lines 2-9), instruction decode logic stage (14 of Fig.3), multiple port register read stage (48/50 of Fig.3), address mode logic stage (see Col.3 lines 2-9), arithmetic logic unit for arithmetic and address calculations stage (see Col.3 lines 50-56), multiple port memory stage (48/50 of Fig.3), branch/wait logic stage (18 of Fig.1), and multiple port register write stage (48/50 of Fig.3). Here, the functions are not shown to be explicit stages of operation in the pipeline, but being that the UltraSparc processor of Parady (see Col.2 lines 66-67) is pipelined (see Col.3 lines 35-43), it is inherent that the operations of these units occur in a pipelined fashion.

Art Unit: 2183

7. Regarding claim 3, Parady has taught a system as recited in claim 1, wherein said processor core supports one or more additional independent groups of at least two processor threads, each group of processor threads being associated with an instruction execution logic mechanism and a memory (see Fig.3).

8. Regarding claim 6, Parady has taught a system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual program threads to identify the particular processor threads on which they are being executed (see Fig.4 and Col.3 line 66 – Col.4 line 8). Here, certain instructions can enable a specific thread upon a thread switch, thus determining the identity of the thread that is desired to be switched to.

9. Regarding claim 7, Parady has taught a system as recited in claim 1, wherein said supervisory control unit (112 of Fig.3) is capable of examining, interpreting, and adjusting the state of the processor core for the purpose of starting and stopping individual processor threads, and modifying the state of each individual processor thread (see Col.3 lines 57-65). Here, the thread switching logic monitors the processing core for a cache miss, and if it determines there was a cache miss, can stop the current thread and start a new thread (see Col.3 lines 57-65), as well as put the threads into interleaving mode (see Col.4 lines 18-29).

10. Regarding claim 9, Parady has taught a system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by one or more controlling threads selected from the processor threads in the processor core, by using input/output instructions to control the operation of one or more processor threads (see Col.3 line 57 – Col.4 line 8). Here, each thread can access the thread switching logic by providing it with a thread ID to switch to upon a long-latency operation which is detected by the thread switching logic, the

Art Unit: 2183

thread ID which can be provided in a load or store (input/output) instruction (see Col.4 lines 5-7).

11. Regarding claim 10, Parady has taught a system as recited in claim 9, wherein said one or more controlling threads are programmable (see Col.3 line 57 – Col.4 line 8). Here, any of the four threads can cause a cache miss to be detected by the thread switching logic (see Col.3 lines 57-65), and can further be programmed to include a thread field that tells the thread switching logic which thread to switch to (see Col.4 lines 1-8).

12. Regarding claim 16, Parady has taught a system as recited in claim 1, wherein said memory is expandable by addition of external memory accessible by the system through said peripheral adaptor (176/180 of Fig.5).

13. Regarding claim 17, Parady has taught a system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core (see Fig.3). Here, the thread switching logic is separate from the core functions of fetch, decode, issue and execute.

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Dickman et al., U.S. Patent No. 4,556,951.

Art Unit: 2183

16. Regarding claim 4, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein the system further comprises a condition code mechanism implemented in said instruction set for detecting specific word data types.

17. However, Dickman has taught a system for detecting specific word data type and setting corresponding condition codes so that conventional program control instructions can be used to control processing, rather than modifying existing control instructions to do so (see Col.2 line 57 – Col.3 line 5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to detect specific types of data words and set their corresponding condition codes so that existing control instructions can be used, thereby creating less work and preserving the previous compatibility of the instruction set.

18. Regarding claim 5, Parady in view of Dickman has taught a system as recited in claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range (see Col.8 line 63 – Col.9 line 12).

19. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 7 above, and further in view of Miyamoto et al., U.S. Patent No. 6,101,569.

20. Regarding claim 8, Parady has taught a system of claim 7, but has not explicitly taught wherein the system further comprises a hardware semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral adaptor and said memory.

21. However, Miyamoto has taught a semaphore vector (see Col.5 lines 34-51) which controls multithread access to peripherals and system memory (see Col.4 line 66 – Col.5 line 33)

Art Unit: 2183

so that data is not inadvertently destroyed by another thread (see Col.1 lines 21-36). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to include the use of hardware semaphore vector to control access to peripherals and memory so that inadvertent data destruction does not take place, and thus incorrect operation does not result.

22. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 9 above, and further in view of Fernando et al., U.S. Patent No. 6,272,616.

23. Regarding claim 11, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said one or more threads are capable of reconfiguring the overall thread processing method of operation so that two or more processor threads can support MIMD operations.

24. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for an instruction that lets the processing threads switch into MIMD mode in order to improve processing performance for a broad range of software types.

25. Regarding claim 12, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said one or more threads can reconfigure the overall thread processing method of operation so that two or more processor threads can support SIMD operations.

Art Unit: 2183

26. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for an instruction that lets the processing threads switch into SIMD mode in order to improve processing performance for a broad range of software types.

27. Regarding claim 13, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said one or more controlling threads are capable of reconfiguring the overall thread processing method of operation so that two or more processor threads can support simultaneously SIMD operations and two or more processor threads can support MIMD operations.

28. However, However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32), which allows SIMD and MIMD modes to be concurrently executing (see Col.12 lines 1-5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for the processing threads to simultaneously execute in both SIMD mode and MIMD mode in order to improve processing performance for a broad range of software types.

Art Unit: 2183

29. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Bishop et al., U.S. Patent No. 5,784,552.

30. Regarding claim 14, Parady has taught the system as recited in claim 1, but has not explicitly taught wherein said supervisory control unit is operable by a first processor thread to start and stop the operation of another processor thread and to examine and alter processor core state information in single-step and multiple-step modes of controlled operation.

31. However, Bishop has taught the execution of an application program under the supervision of a debugging program, the debugging program which halts the application program (see Col.5 lines 11-22) and can examine and alter state information via debugging instruction execution in either single-step or multi-step modes of debugging (see Col.7 lines 13-45) so that an application programmer can more thoroughly test and debug their programs in a controlled testing environment (see Col.1 lines 17-35). One of ordinary skill in the art would have recognized that thoroughly tested and debugged programs are less likely to fail and provide incorrect results. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow a debugging program to stop and start another program so that instructions in the other program can be thoroughly tested and debugged in both single-step and multi-step modes of debugging.

32. Claims 15 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Zammit et al., European Patent Application No. 1091292.

Art Unit: 2183

33. Regarding claims 15 and 19-20, Parady has taught a system as recited in claim 1, but has not explicitly taught

- a. Wherein the system further comprising an identifying bit pattern embedded in the instruction set (Applicant's claim 15);
- b. Wherein said identifying bit pattern is used to identify programming code for code protection purposes (Applicant's claim 19); and
- c. Wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism (Applicant's claim 20).

34. However, Zammit has taught a processor which identifies values in unused bit fields of instruction during a conversion so that the unused bit fields which contain inappropriate values, which could result in incorrect translation, can be corrected before being executed (see p.3 lines 9-16, 35-39). This bit pattern also protects programming code from being incorrectly translated and causing incorrect execution of the program code. This bit pattern also does not affect the instruction execution logic operation, since it is only used to identify whether there are unused bit fields, which contain inappropriate values, and does not cause the execution logic to perform differently from what the instruction intended. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to identify values of unused bits so that inappropriate values are not incorrectly translated, and thus incorrect execution does not occur.

35. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Wilske, U.S. Patent No. 4,155,115.

Art Unit: 2183

36. Regarding claim 18, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein said peripheral adaptor is capable of controlling analog and digital processing functions.

37. However, Wilske has taught a microprocessor system which has a peripheral controller capable of receiving and controlling inputs from both analog and digital sources (see Col.2 lines 7-34) so that both types of sources can be controlled from one location in order to reduce cost and lessen hardware (see Col.1 lines 14-24). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow its peripheral adapter to control both analog and digital sources so that the amount of hardware needed to control both types of sources can be reduced, thus lowering cost.

***Response to Arguments***

38. Examiner withdraws the objections to the specification in favor of the amended specification.

39. Examiner withdraws the claim objections and 35 U.S.C. § 112, second paragraph in favor of the amended claims.

40. Applicant's arguments filed 16 October 2004 have been fully considered but they are not persuasive.

41. Applicant argues in essence on pages 20-21,

“...The most fundamental distinction between Parady and the present invention is that the present invention executes multiple threads of an application program using multithreaded processor *hardware* – i.e., a multithread processor core

comprising at least four independent processor threads – a feature that Parady neither teaches nor suggests.

...However, it is readily apparent from Figure 3 in Parady (as described at Col. 3, lines 35-43) that the multithreaded aspect of the Parady invention is software0based rather than hardware-based as in the present invention...”

42. This has not been found persuasive. It does not matter whether the invention is implemented in hardware or software. They are functionally equivalent and, if something is implemented in software, it can be implemented in hardware. The same is true for the reverse. If something is implemented in hardware, it can be implemented in software. This is known in the art and is taught by Andrew Tanenbaum’s Structured Computer Organization Second Edition on page 11, paragraphs 2-3.

43. Applicant argues in essence on page 21-22

“...The present invention enables *simultaneous* execution of multiple program threads using a single processor core, whereas simultaneous execution of multiple program threads using the Parady technology would be possible only by incorporating additional processor cores such that a separate core would be dedicated to each program thread.”

44. This has not been found persuasive. Parady teaches in column 1, lines 11-20 that multi-threading systems run two or more programs at the same time and multiple actions are processed concurrently in multi-threading. Parady’s system is a multi-threaded system and multi-threaded systems are capable simultaneous execution. Simultaneous execution, in the broadest interpretation, means that the execution occurs at the same time.

***Conclusion***

45. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

46. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

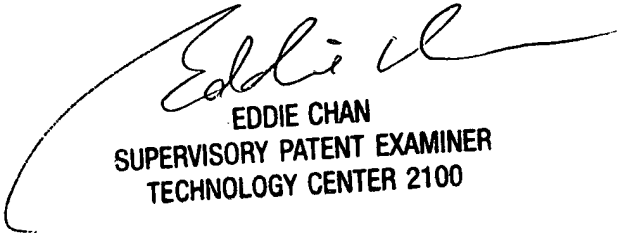
47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

48. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2183

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL  
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7 January 2005



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